REMARKS

Claims 34-42 are in the application. Claims 1-33 have been cancelled.

By this amendment, applicants have amended claim 1. FIG. 4 supports the changes made to claim 1.

Response to 35 U.S.C. §102 Rejections

Claims 34 and 38-41 were rejected under 35 U.S.C. §102(e) as being anticipated by Lur et al., USP 5,640,041. This rejection is traversed in view of the amendments made herein and the remarks presented hereinafter.

Claim 34 calls for, among other things, an intermediary of a semiconductor device including a pillar region comprising a dielectric material formed in the first recessed region and extending from the lower surface, wherein a void region is formed within the pillar region. Claim 34 also calls for a polysilicon cap layer having a lower surface formed adjoining upper surfaces of the pillar region, wherein the lower surface is aligned with the void region, and wherein sidewall surfaces of the pillar region are devoid of the polysilicon cap layer, and wherein the pillar region, the polysilicon cap layer and the void region are configured to form an isolation region having reduced substrate capacitance.

Applicants respectfully submit that Lur does not show a polysilicon cap layer having a lower surface formed adjoining upper surfaces of the pillar region, wherein the lower surface is aligned with the void region. Thus, for

at least these reasons, applicants respectfully submit that claim 34 is allowable.

Claims 38-41 depend from claim 34 and are believed allowable for at least the same reasons as claim 34.

Claims 35-37 and 42 were rejected under 35 U.S.C. §103(a) as being unpatentable over Lur. In view of the arguments presented above and the dependence of these claims on claim 34, applicants respectfully submit that claims 35-37 and 42 are allowable over Lur for at least the same reasons as claim 34.

In view of the above, it is believed that the claims are allowable, and the case is now in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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